

# A Direct Digital Synthesizer with an On-Chip D/A-Converter

Jouko Vankka, *Student Member, IEEE*, Mikko Waltari, *Student Member, IEEE*, Marko Kosunen, and Kari A. I. Halonen

**Abstract**—A direct digital synthesizer (DDS) with an on-chip D/A converter is designed and processed in a 0.8- $\mu\text{m}$  BiCMOS. The on-chip D/A converter avoids delays and line loading caused by interchip connections. At the 150-MHz clock frequency, the spurious free dynamic range (SFDR) is better than 60 dBc at low synthesized frequencies, decreasing to 52 dBc worst case at high synthesized frequencies in the output frequency band (0–75 MHz). The DDS covers a bandwidth from dc to 75 MHz in steps of 0.0349 Hz with the frequency switching speed of 140 ns. The chip has a complexity of 19 100 transistors with a die/core area of 12.2/3.9 mm<sup>2</sup>. The power dissipation is 0.6 W at 150 MHz @ 5 V. The maximum operating clock frequency of the chip is 170 MHz.

**Index Terms**—BiCMOS integrated circuits, direct digital synthesizers, frequency synthesizers, mixed analog–digital integrated circuits, on-chip digital-to-analog converter, read only memories.

## I. INTRODUCTION

TRADITIONAL designs of high bandwidth frequency synthesizers employ the use of a phase-locked-loop (PLL). A direct digital synthesizer (DDS) provides many significant advantages over PLL approaches. Fast settling time, sub-Hertz frequency resolution, continuous-phase switching response, and low phase noise are features easily obtainable in DDS systems. Although the principle of the DDS has been known for many years [1], the DDS did not play a dominant role in wideband frequency generation until recent years. Earlier DDS's were limited to produce narrow bands of closely spaced frequencies, due to limitations of digital logic and D/A-converter technologies. Recent advantages in IC technologies have brought about remarkable process in this area.

The architecture used in this design was originally introduced in [1]. The block diagram of the DDS is shown in Fig. 1. The input word (frequency control word) to the phase accumulator controls the frequency of the generated sine wave. The phase value is generated by using the modulo  $2^j$  overflowing property of a  $j$ -bit phase accumulator. The rate of the overflow is the output frequency

$$f_{\text{out}} = \frac{F_r f_{\text{clk}}}{2^j} \quad \forall F_r < 2^{j-1} \quad (1)$$

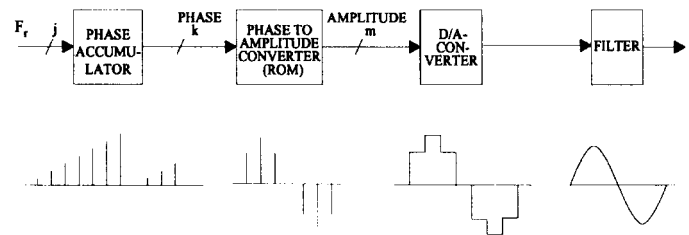


Fig. 1. Simplified block diagram of the direct digital synthesizer and the signal flow in the DDS.

where  $F_r$  is the frequency control word,  $j$  is the phase accumulator word length,  $f_{\text{clk}}$  is the clock frequency, and  $f_{\text{out}}$  is the output frequency. The constraint in (1) comes from the sampling theorem. The frequency control word in (1) is an integer, therefore the frequency resolution is found by setting  $F_r = 1$

$$\Delta f = \frac{f_{\text{clk}}}{2^j}. \quad (2)$$

The phase accumulator addresses the sine ROM which converts the phase information into the values of a sine wave. The ROM output is presented to the D/A converter, which develops a quantized analog sine wave. The filter removes high-frequency sampling components and provides a pure sine wave output. As the DDS generates frequencies close to one half the clock frequency, the first image becomes more difficult to filter. Therefore, in practice, the DDS operation is limited to approximately 40% of the clock frequency.

In [2]–[4], digital parts of the DDS have been implemented with CMOS technology in one chip, and the off-chip D/A converter is a bipolar or GaAs device. It is quite easy to increase the operating speed of the CMOS DDS up to 800 MHz by parallel architectures [4]. The D/A converter is the bottleneck in the CMOS design, because the spectral degradation due to incomplete settling of the output and other dynamic effects restrict the operating speed of the D/A converter below the digital part. A CMOS DDS with an on-chip D/A converter has been reported with the operating clock frequency of 50 MHz fabricated in 1.0- $\mu\text{m}$  CMOS [5]. A bipolar DDS with an on-chip D/A converter has been reported with the output bandwidth of 500 MHz fabricated in 1.0- $\mu\text{m}$  silicon bipolar process with “trench” isolation [6]. The power consumption of this device is 5 W in the sine wave output mode [6]. The DDS presented in this paper is designed and processed in BiCMOS, which allows CMOS logic functions of low power and high density to be produced on the same chip with a high-speed BiCMOS D/A converter.

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TABLE I  
MEMORY COMPRESSION AND ALGORITHMIC TECHNIQUES IN A CASE OF 12-B PHASE TO 10-B AMPLITUDE MAPPING

Method	Needed ROM	Total compression ratio	Additional circuits (not includes quarter wave logic†)	Worst case spur (below carrier)	Comments
Uncompressed memory	$2^{12} \times 10$ bits	1 : 1	-	-81.76 dBc	reference
Mod. Sunderland architecture	$2^7 \times 7$ bits $2^7 \times 3$ bits	32 : 1	adder†† adder	-73.59 dBc	simple
Mod. Nicholas architecture	$2^7 \times 7$ bits $2^7 \times 3$ bits	32 : 1	adder†† adder	-74.56 dBc	simple
Taylor series approximation with two terms	$2^6 \times 7$ bits $2^6 \times 5$ bits	53 : 1	adder†† adder multiplier	-73.28 dBc	need multiplier
CORDIC algorithm	-	-	12 pipelined stages, 16-bit inner word length	-73.32 dBc	much computation

† Using the quarter wave symmetry of sine function, complementors must be used to take the absolute value of the quarter phase and multiply the output of the sine look-up table by -1 (see Fig. 2).

†† The word length of the sine ROM is shortened by 2-bit, because the sine ROM stores the difference between sine amplitude and phase. The penalty is an extra adder at the output of the sine ROM.

## II. APPLICATIONS AND DESIGN REQUIREMENTS

Applications for DDS's range from instrumentation and measurement to modern digital communications. This DDS is primarily intended for frequency agile communication systems, where fast frequency switching speed and fine frequency resolution of synthesizers are important. The primary considerations in the design of this DDS were a fine frequency resolution, spectral purity, and low power dissipation.

This chip was based on a 0.8- $\mu\text{m}$  double-metal double-poly BiCMOS process. The wordlength of the on-chip D/A converter was selected to be 10 b. Extra bits give no benefits at high output and clock frequencies, because dynamic nonlinearities dominate the D/A converter output spectrum. To meet the distortion requirements of the 10-b D/A converter, the maximum clock frequency is limited to 150 MHz. The phase accumulator word length was chosen to be 32 b to achieve a frequency resolution of 0.0349 Hz at the clock rate of 150 MHz according to (2). Since the amount of memory required to encode the entire width of the phase accumulator would be prohibitive, only 12 of the most significant bits of the accumulator output are used to calculate the sine-wave samples. The phase resolution of 12 b results in a spurious performance due to the phase accumulator truncation of -72 dBc [7], which will be below the spur level of the 10-b D/A converter at 150 MHz.

## III. SINE MEMORY COMPRESSION

A straightforward implementation of the sine memory requires a  $2^{12} \times 10$ -b ROM, whose access time reduces the

maximum DDS clock frequency much below 150 MHz. Therefore, a sine memory compression technique is applied to reduce the size and access time of the sine ROM [7].

The most elementary technique of the sine memory compression is to store only the  $\pi/2$  rad of sine information, and to generate the ROM samples for the full range of  $2\pi$  by exploiting the quarter-wave symmetry of the sine function. Beyond that, the methods of compressing the quarter wave memory include: the trigonometric identity [8], the Nicholas method [7], the use of Taylor series [9], and the CORDIC algorithm [10]. A computer program has been created to simulate the effects of the memory compression and algorithmic techniques on the output spectrum of the DDS. In the case of 12-b phase to 10-b amplitude mapping, Table I shows how much memory and how many additional circuits are needed in each memory compression and algorithmic technique to meet the spectral requirement for the worst case spur level, which is about -73 dBc due to the sine memory compression. The spur level (-73 dBc) will stay below the spur level of the 10-b D/A converter at 150 MHz. The best compression ratio is given by the Taylor series approximation, but a multiplier is needed. The problem of the CORDIC algorithm is in the hardware complexity. In this design, the Mod. Nicholas architecture is used, because it gives lower worst case spur level than the Sunderland architecture with the same hardware complexity.

### A. Exploitation of Sine Function Symmetry

Due to the symmetry of the sine function, only a quarter of the full samples are stored in the sine look-up table. The

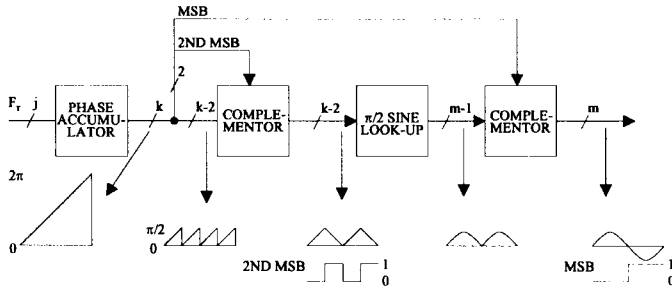
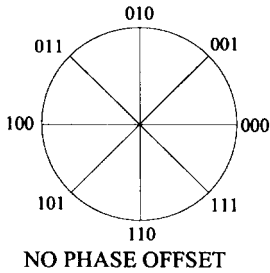


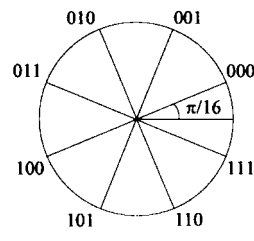
Fig. 2. Logic to exploit quarter wave symmetry.

### THE PHASE ADDRESS (k) IN THE THREE BIT CASE



NO PHASE OFFSET

### THE PHASE ADDRESS (k) IN THE THREE BIT CASE



PHASE OFFSET

Fig. 3. A 1/2-LSB phase offset is introduced in all phase addresses. In this case, 1/2 LSB corresponds to  $\pi/16$ . The 1/2-LSB phase offset is added to all the sine lookup table samples. In this figure it is shown that one's complementor maps the phase values to the first quadrant without error.

full wave output can be recovered by inverting the phase and amplitude appropriately, as shown in Fig. 2. In most practical DDS implementations, numbers are represented in the two's complement format. Therefore, the two's complementing must be used to take the absolute value of the quarter phase and multiply the output of the look-up table by  $-1$ . However, it can be shown that if a 1/2-least-significant-bit (LSB) offset is introduced into a number that is to be complemented, then a one's complementor may be used in the place of two's complementor without introducing an error [7]. This provides savings in hardware since a one's complementor may be implemented as a set of simple exclusive-OR gates. This 1/2-LSB offset is provided by choosing the look-up table samples so that there is a 1/2-LSB offset in both the phase and amplitude of the samples [7], as shown in Figs. 3 and 4.

### B. Compression of the Quarter-Wave Sine Function

The phase address of the quarter of the sine wave is defined as  $P = a + b + c$ , with the wordlength of the variable  $a$  to be  $A$ , the wordlength of  $b$  to be  $B$ , and  $c$  to be  $C$ . In Fig. 5, the variables  $a, b$  form the coarse ROM address, and the variables  $a, c$  form the fine ROM address. In Fig. 6, the coarse ROM samples are represented by the dot along the dashed line, and the fine ROM samples are chosen to be the difference between the value of the sine function along the dashed line and the value of the coarse ROM samples. In Fig. 6, the function is divided into four regions, corresponding to  $a = 00, 01, 10$ , and  $11$ . Within each region, only one interpolation value may be used between the sine function along the dashed line and the coarse ROM samples for all

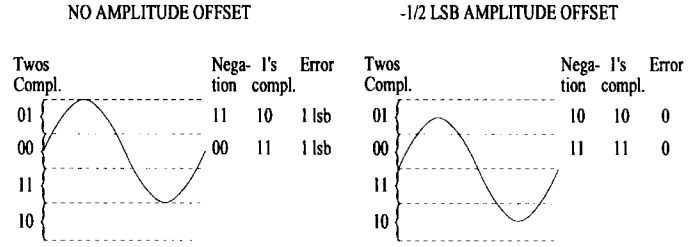


Fig. 4. A  $-1/2$ -LSB offset is introduced into the amplitude that is to be complemented; then the negation can be carried out with one's complementor without error in Fig. 2. There must be a  $+1/2$ -LSB offset in the D/A-converter output.

the same  $c$  values. The interpolation value used for each value of  $c$  is chosen to minimize either the mean square or the maximum absolute error of the interpolation within the region [7]. Computer simulations determined that the optimum partitioning of the ROM address word lengths to provide a 10-b phase resolution was  $A = 4$ ,  $B = 3$ , and  $C = 3$ , using the notation in Fig. 5. Simulations showed that the mean square criterion gives nearly the same maximum spur level as the minimum-maximum error criterion in this segmentation. In Fig. 5, the size of the upper memory, whose access time is the most critical, is reduced by the sine difference algorithm [7]. This saves 2 b of amplitude in the storage of the sine function, but an extra adder is required at the coarse ROM output [7]. The architecture for this ROM compression technique is shown in Fig. 5. The  $2^{12} \times 10$  sine samples are compressed into  $2^7 \times 7$  coarse samples and  $2^7 \times 3$  fine samples resulting in a compressing ratio of 32:1.

## IV. PHASE ACCUMULATOR

In practice, the phase accumulator circuit cannot complete the 32-b addition in a short single clock period because of the delay caused by the carry bits propagating through the adder. In order to enhance the operation to higher clock frequencies, one solution is a pipelined accumulator [11], shown in Fig. 7. To reduce the number of gate delays, a kernel 4-b adder is used in Fig. 7, and the carry is latched between successive adder stages. In this way, the length of the accumulator does not reduce the maximum operating speed, but the penalty is that the tuning latency increases. To maintain the valid accumulator phase during the frequency control word transition, the new frequency control word is moved into the pipeline through the delay circuit. The D-flip-flop (DFF) circuits in the input delay equalization demand substantial circuit area and power and would impact the loading of the clock distribution network.

The output delay circuitry is essentially identical to the input delay equalization circuitry, inverted so that the low order bits have a maximum delay while the most significant bits have the minimum delay. The 12 most significant phase bits are used to calculate the sine function. Therefore, only these 12 b are delayed in Fig. 7.

In Fig. 7, for  $RESET = 1$ , the carry input toggles periodically between zero and one, with the effect of adding 1/2 LSB weight to the phase accumulator. This modifies the existing  $j$ -bit phase accumulator structure to emulate the operation of a phase accumulator with a word length of  $j + 1$  bits under



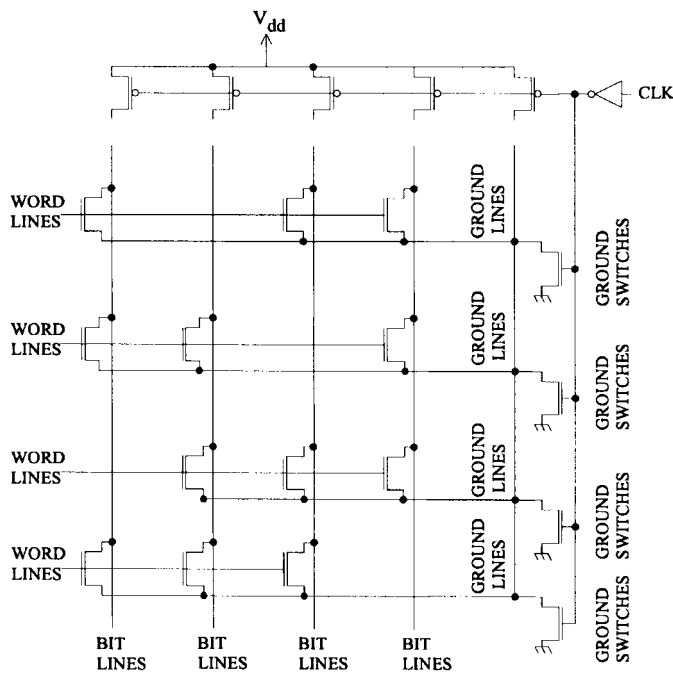


Fig. 9. ROM memory points matrix.

lines. The memory works as follows: during precharge—high level of the clock—all the bit lines are pulled up. The evaluating phase occurs when the clock goes low, hence conditionally discharging the bit lines. The word decoder selects a single word line, then transistors with the gate connected to that word line will turn on. Adding the ground switches between the transistors and the ground makes it possible to select the word line during the precharging. This increases the operation speed of the memory at the expense of some power dissipation, because the power consumption is increased due to the precharging and discharging the ground lines at every clock cycle. If there is a transistor in the intersection of the bit line and the selected word line, the ground switch will pull down the bit line to the ground when the clock goes low. If the transistor is absent, the bit line will remain high.

### B. D/A-Converter

The designed IC has an on-chip D/A converter, which avoids delays and line loading caused by interchip connections. This D/A converter is based on a well-known weighted current array. The block diagram of the two-stage current array D/A converter is shown in Fig. 10. The input to the D/A converter is converted into a differential emitter coupled logic (ECL) signal. One stage of latches has been inserted between the CMOS/ECL converter and the current switches to enhance the switching speed and ensure simultaneous switching of all bits. The ten binary-weighted currents are switched to either the output branch or the complementary output branch by current switches. The output currents are converted into voltages with resistors. Finally, there is an emitter follower buffering the output. The D/A converter is implemented with a balanced design, which results in reduced even-order distortion and provides common-mode rejection to disturbances.

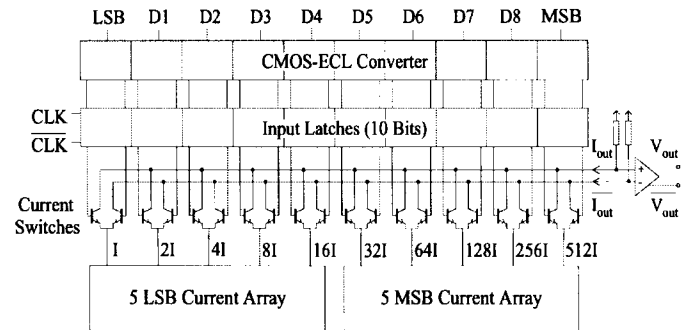


Fig. 10. A 10-b two-stage current array D/A converter.

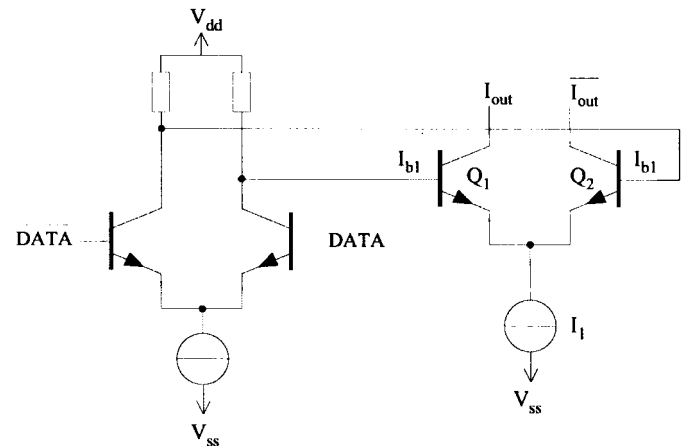


Fig. 11. D-flip-flop output buffer and bipolar current switch.

In the two-stage weighted current array, only 31 most significant bit (MSB) and 31 LSB equivalent unit current sources are required for a 10-b D/A converter. This structure saves 961 unit current sources (from 1023 to 62) compared to the straightforward current source configuration constructed from unit current sources. The reduced number of unit current sources makes it possible to design the current source transistors large to achieve good tolerance against uncorrelated process variations, but still maintain the array sufficiently small to keep the mismatch due to the correlated process variations below the required level. The cascode structure is used to increase the output impedance of the unit current source, which improves the linearity of the D/A converter.

The latches are implemented by differential current-mode logic (DCML) D-flip-flops, which is faster than ECL-type D-flip-flops. Fig. 11 shows a D-flip-flop output buffer and a current switch for a single bit section. The bipolar current switch steers the current  $I_1$  between the two output branches. The current switch is connected to the output of the D-flip-flop buffer at the left-hand side of Fig. 11. The D-flip-flop output buffer limits the control voltage swing and buffers between the input digital signal and the current switch.

In the process used, the MOS current switch cannot toggle the current between the complementary outputs at the clock rate of 150 MHz, so the bipolar current switch is used. Furthermore, the required control voltage swing at the input of the bipolar current switch is much lower compared to the required control voltage swing of a MOS current switch for

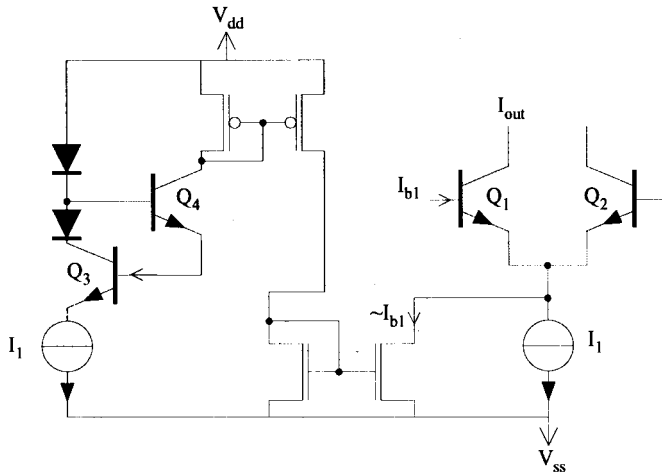


Fig. 12. The base current compensation.

a practical design. The problem of the bipolar switches is the error in the output current due to the finite forward current gain of the switch transistors. In Fig. 11, the actual current  $I_{out}$  delivered to the output branch differs from the actual bit current  $I_1$  by an amount equal to the base current  $I_{b1}$  of the transistor  $Q_1$

$$I_{out} = I_1 - I_{b1} = \frac{1}{1 + \frac{1}{\beta_F}} I_1 \quad (3)$$

where  $\beta_F$  is the forward current gain of  $Q_1$ . This would only cause gain error (not errors in linearity) if the forward current gain of the transistors in all switching pairs were equal. Actually, the forward current gain depends on the magnitude of the current and the temperature, which vary over the current switches. Therefore, the base currents have to be compensated to reduce linearity errors caused by variations in the forward current gain over bipolar current switch transistors. A simple way of minimizing the error is to use a Darlington-connected pair of transistors. Although this is used in some designs [14], it tends to degrade the switching speed of the circuit significantly. In Fig. 12, the idea of the base current compensation is to predistort the current of the binary current source ( $I_1$ ) by a current, which is equal to the base current of the current switch. In the base current compensation circuit, a binary-weighted amount of current ( $I_1$ ) is driven through a bipolar transistor ( $Q_3$ ), whose geometrical size is identical to the current switch transistor ( $Q_1$ ). The operating point of the transistor  $Q_3$  is set the same as in the switch transistor  $Q_1$  by a transistor ( $Q_4$ ) and two diodes. Therefore, the base current of the transistor ( $Q_3$ ) is almost same as in the current switch transistor ( $Q_1$ ). This current is mirrored with MOS current mirrors at the common emitter node of the current switches. With the base current compensation circuit, the output current of the current switch transistor is approximately (see Appendix)

$$I_{out} \approx \frac{1}{2} \frac{1}{1 + \frac{1}{\beta_F}} I_1. \quad (4)$$

TABLE II  
POWER CONSUMPTION AND MAXIMUM OPERATION FREQUENCY OF  
DDS BLOCKS BASED ON SPICE SIMULATIONS AT 25°C

Block of DDS	Power Consumption	Maximum Operation Frequency
Phase Accumulator	120 mW @ 5 V	150 MHz @ 5 V
	40 mW @ 3.3 V	110 MHz @ 3.3 V
Additional Logic	200 mW @ 5 V	160 MHz @ 5 V
	72 mW @ 3.3 V	114 MHz @ 3.3 V
ROM's	140 mW @ 5 V	330 MHz @ 5 V
	50 mW @ 3.3 V	200 MHz @ 3.3 V
D/A-Converter	120 mW @ 3.3 V	250 MHz @ 3.3 V†
DDS Circuit	0.6 W at 150 MHz @ 5 V	150 MHz @ 5 V
	0.282 W at 110 MHz @ 3.3 V	110 MHz @ 3.3 V

† The load capacitance  $C_L = 10$  pF.

Comparing (3) and (4), the error due to the finite  $\beta_F$  has been reduced from  $1/\beta_F$  to  $2/\beta_F^2$ . According to the simulations, the base current compensation circuit has a negligible effect on the speed of the D/A converter.

### C. Summary of DDS Block Design

The digital parts of the chip are implemented with CMOS design to reduce power consumption. The 10-b D/A converter is designed with BiCMOS technology in order to operate at a clock rate of 150 MHz. Table II shows the simulated power consumption and maximum clock frequencies for each DDS block. In Table II, the bottleneck of this DDS is the phase accumulator operation speed of 150 MHz. It is quite easy to increase the operation speed of the phase accumulator and the additional logic by pipelining. But, to meet the distortion requirements of the 10-bit D/A converter, the maximum clock frequency of the DDS is limited to 150 MHz. For low power consumption applications, by reducing the supply voltage of the DDS, the power consumption can be decreased from 0.6 to 0.28 W, but the maximum clock frequency is decreased from 150 to 110 MHz (see Table II).

### D. Layout Considerations

A problem inherent in high-speed CMOS chips is the power supply switching noise. To minimize the coupling of the switching noise from the digital logic to the output of the D/A converter, the power supplies of the digital logic and the analog part are routed separately. Horizontal and vertical shielding between the analog signals routing and digital data lines have been used to minimize coupling between these. All digital blocks are surrounded by guard rings and the analog parts of the D/A converter by double guard rings to minimize noise injected to the analog output through the substrate. Separate pads connect the guardrings to the off-chip ground. The most efficient way to decrease the noise coupling through the substrate is to reduce the inductance between the ground and the substrate [15]. In this circuit, this inductance is small, because the ground level is connected through several bonding wires and package pins.

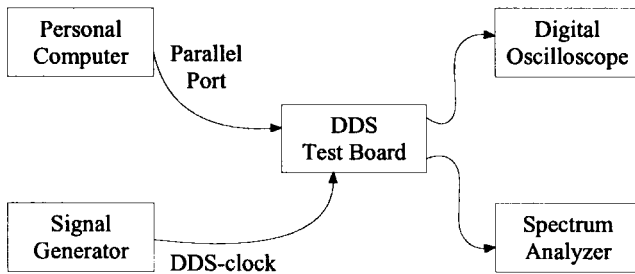


Fig. 13. The DDS test system.

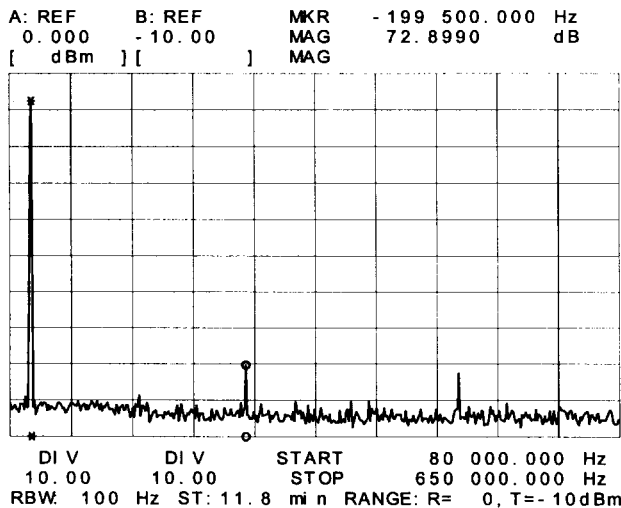


Fig. 14. Spectrum of 0.1-MHz output sine wave, where the clock frequency is 150 MHz.

To eliminate process- and temperature-related gradients in the D/A converter current source transistor arrays, a common-centroid layout is used [16]. The D/A converter clock controls the latches that drive the output current switches. Therefore, it controls the digital-to-analog conversion process and must be considered an analog signal. Its purity has a direct effect on the output spurs. In the layout, the D/A converter clock signal is separated from the digital signals to prevent the switching currents from coupling onto the D/A converter clock.

## VI. EXPERIMENTAL RESULTS

To evaluate the DDS chip, a test board was built and a computer program was developed to control the measurement. In the software, the frequency control word could be written in HEX or in the required frequency in MHz. In the latter case the software will calculate the corresponding frequency control word. The frequency control word and the other of the control signals are loaded into the test board via the parallel port of a personal computer. The block diagram of Fig. 13 illustrates the DDS test system.

The effect of D/A-converter static nonlinearities is investigated in Fig. 14, where the clock frequency is 150 MHz and the output frequency is low. Even-order distortion is reduced due to the balanced operation. The spurious free dynamic range (SFDR) is 72.9 dBc in Fig. 14, where the worst spurs are the third and fifth harmonics. The D/A converter fulfills the requirement of a 10-b static linearity.

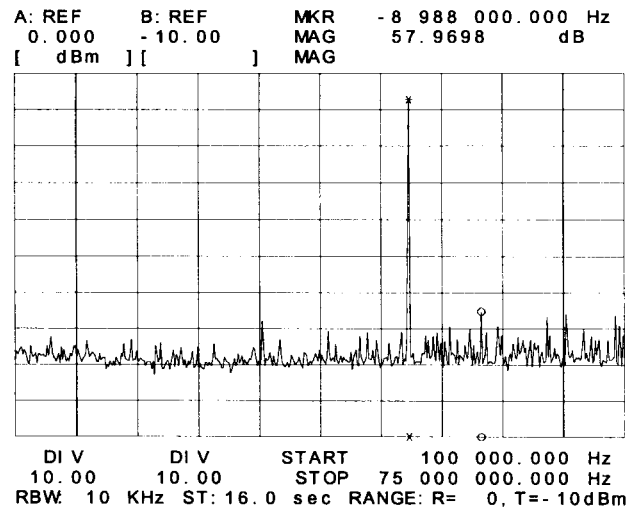
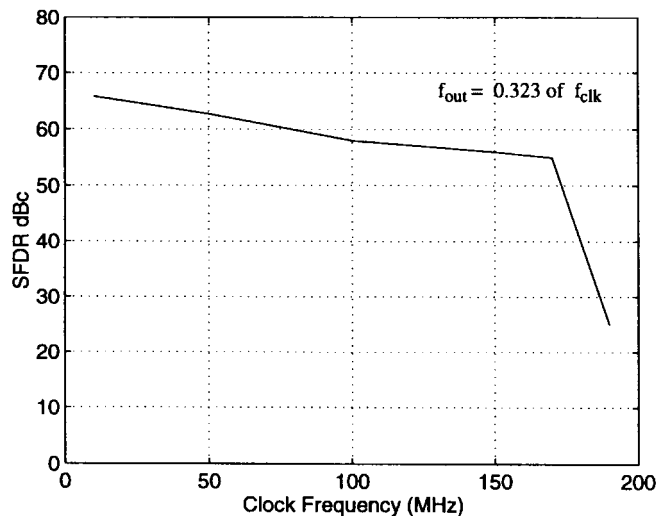


Fig. 15. Spectrum of 48.5-MHz output sine wave, where the clock frequency is 150 MHz.

Fig. 16. SFDR as a function of clock frequency, for  $f_{out} = 0.323$  of  $f_{clk}$ .

A DDS's worst case close to carrier spurs at wideband (Nyquist bandwidth = dc to  $f_{clk}/2$ ) typically occur when the output frequency is tuned close to  $f_{clk}/4$  or  $f_{clk}/3$ . The measured SFDR was 57.9 dBc at a generated frequency of 48.5 MHz in Fig. 15, where the clock frequency is 150 MHz. The worst case spur is the fifth aliased harmonic at 57.5 MHz ( $2 \times f_{clk} - 5 \times f_{out}$ ). Fig. 16 shows SFDR as a function of clock frequency, for  $f_{out} = 0.323$  of  $f_{clk}$ . The frequency control word was set constant  $(52C5F92C)_{16}$ , and the clock frequency was swept over a range of frequencies from 10–190 MHz. From Fig. 16, it can be seen that with this frequency control word, the DDS operates to 170 MHz clock frequency, after which it no longer produced a sine-wave at the output due to internal timing problems.

Fig. 17 shows SFDR as a function of output frequency for a fixed clock frequency. At the 150-MHz clock frequency, the SFDR is better than 60 dBc at low synthesized frequencies, decreasing to 52 dBc at high synthesized frequencies in the output frequency band as shown in Fig. 17. In the high

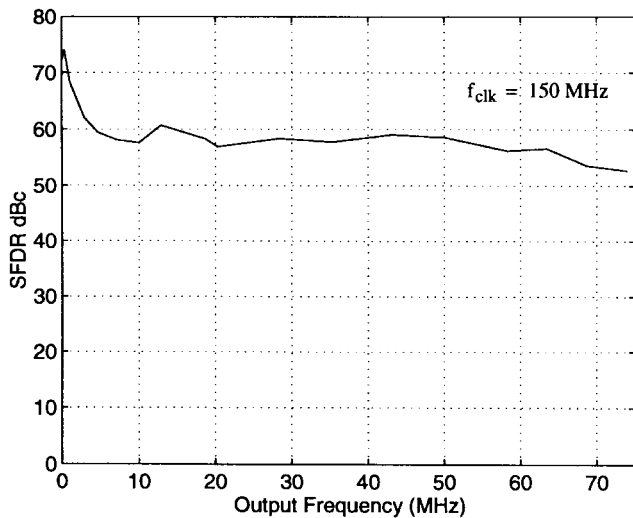


Fig. 17. SFDR as a function of output frequency, for  $f_{clk} = 150$  MHz.

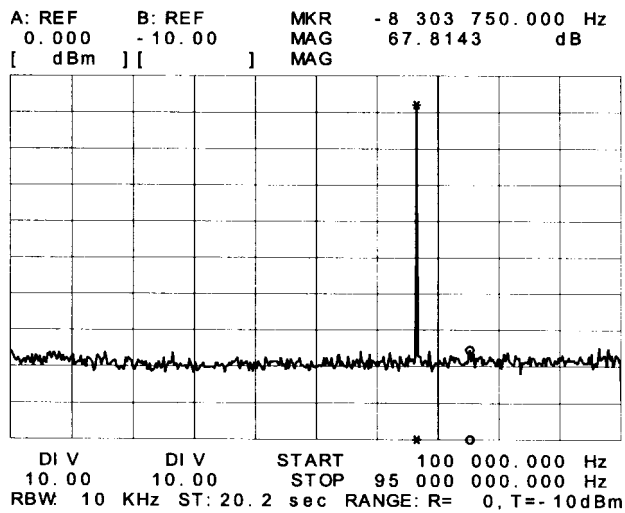


Fig. 18. Spectrum of 63 1/3-MHz output sinewave, where the clock frequency is 190 MHz.

synthesized frequencies, there will be output frequencies where the SFDR is very good. For example, Fig. 18 illustrates a spectrum plot of 63 1/3-MHz output sinewave, where the clock frequency is 190 MHz. In this case, the aliased harmonics fall down to the generated frequency, therefore the SFDR is better than 68 dBc.

The power consumption of the DDS chip agrees with simulated results of the Table II. Typically, the DDS operates up to the clock frequency of 190 MHz after which errors will occur due to the internal timing problems. However, in some frequency control words these errors will already occur at the clock rate of 180 MHz, so the maximum operating clock frequency is 170 MHz.

In the DDS, the close-in phase noise is determined by the purity of the clock source. The DDS divides the clock frequency by some real number. Therefore, the close-in phase noise is reduced by  $20 \times \log_{10}(N)$ , where  $N$  is a division ratio between the DDS clock and output frequency. Of course, the DDS circuitry has a noise floor which at some point will

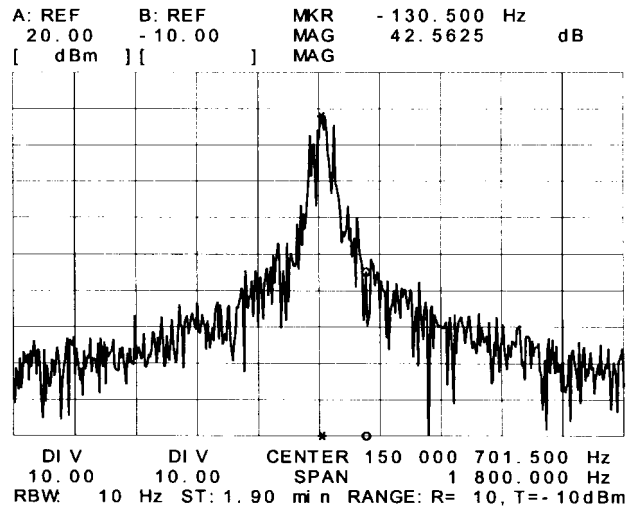


Fig. 19. The close-in spectrum of the clock source at 150 MHz.

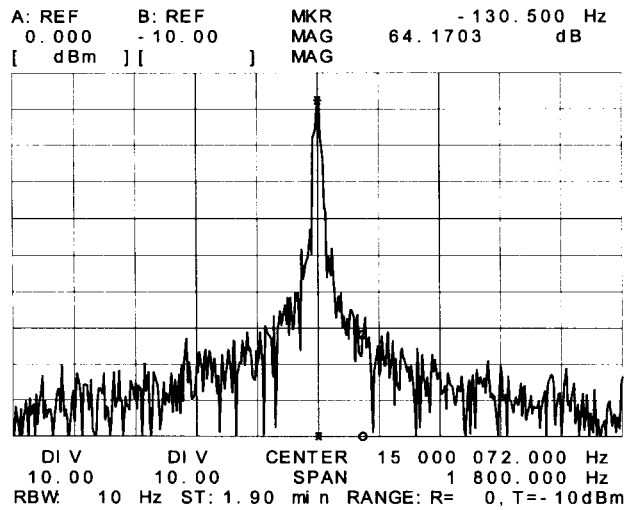


Fig. 20. The close-in spectrum of the 15-MHz output sinewave where the clock frequency is 150 MHz.

limit this improvement. Fig. 19 shows the spectrum of the clock source at 150 MHz. Fig. 20 shows the spectrum of the 15-MHz output sine wave where the clock frequency is 150 MHz. The relative phase noise level should improve by 20 dB [ $20 \times \log_{10}(10)$ ]. The relative power level of the phase noise at offset 130 kHz from the carrier is about 42.5 dBc in Fig. 19 and 64.2 dBc in Fig. 20. The relative improvement in the close-in phase noise agrees with the theory.

## VII. CONCLUSIONS

The DDS with an on-chip D/A converter covers a bandwidth from dc to 75 MHz in steps of 0.0349 Hz with the frequency switching speed of 140 ns. The on-chip D/A converter avoids delays and line loading caused by interchip connections. The two-stage current array D/A converter reduces the number of the current sources and thus simplifies the connection among these current sources and makes more efficient use of the chip area. At the 150-MHz clock frequency, the SFDR is better than 60 dBc at low synthesized frequencies, decreasing

TABLE III  
DDS CHIP SPECIFICATIONS

IC Technology	0.8 $\mu\text{m}$ double-metal double-poly BiCMOS
Max Clock Frequency	170 MHz @ 5 V
Tuning Bandwidth	75 MHz (0.5 $\times$ 150 MHz)
Frequency Resolution	0.0349 Hz (at 150 MHz)
Frequency Switching Time	140 ns (21 $\times$ 1/(150 MHz))
SFDR at low $f_{\text{out}}$	> 60 dBc (at 150 MHz)
SFDR at high $f_{\text{out}}$	> 52 dBc (at 150 MHz)
Transistor Count	19,100
Power Dissipation ( $f_{\text{out}} = f_{\text{clk}}/3$ )	0.6 W at 150 MHz @ 5 V
Die/Core Size	12.2 mm <sup>2</sup> /3.9 mm <sup>2</sup>

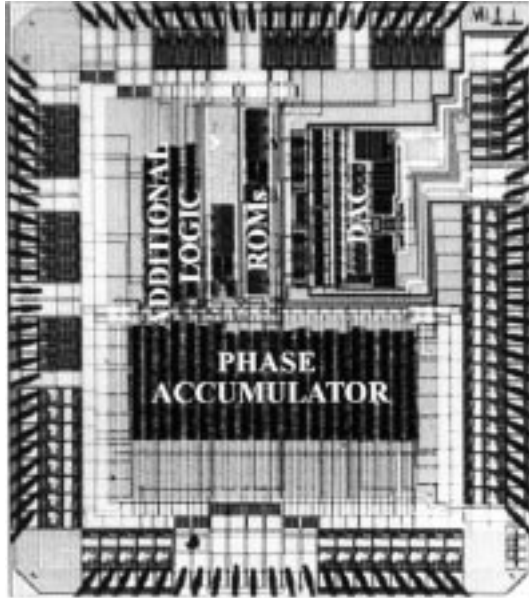


Fig. 21. The photomicrograph of the chip.

to 52 dBc worst case at high synthesized frequencies in the output frequency band (0–75 MHz). Table III summarizes chip specifications. Fig. 21 shows the photomicrograph of the chip. This chip provides the fast frequency switching speed, fine frequency resolution, and low power consumption, which are the key properties in many frequency agile communication systems.

#### APPENDIX

##### DERIVATION OUTPUT CURRENT OF THE BIPOLAR CURRENT SWITCH WITH BASE CURRENT COMPENSATION

In the base current compensation circuit (Fig. 12), a binary weighted amount of current ( $I_1$ ) is driven through a bipolar transistor ( $Q_3$ ), whose geometrical size is identical to the current switch transistor ( $Q_1$ ). The operating point of the transistor ( $Q_3$ ) is set to be the same as in the switch transistor ( $Q_1$ ) by a transistor ( $Q_4$ ) and two diodes. Therefore, the forward current gain of the transistor ( $Q_3$ ) is the same as in the current switch transistor ( $Q_1$ ). The base current of the transistor ( $Q_3$ ) is

$$I_{b3} = \frac{I_1}{1 + \beta_F} \quad (5)$$

where  $\beta_F$  is the forward current gain of the transistor ( $Q_3$ ). The collector current of the cascode transistor ( $Q_4$ ) is

$$I_{C4} = \frac{I_{b3}\beta_{F4}}{1 + \beta_{F4}} = \frac{\beta_{F4}}{(1 + \beta_{F4})(1 + \beta_F)} I_1 \quad (6)$$

where  $\beta_{F4}$  is the forward current gain of ( $Q_4$ ). The collector current of the transistor ( $Q_4$ ) is mirrored with MOS current mirrors at the node of the current switches. If the current mirrors are assumed ideal, then the emitter current of the current switch transistor is

$$I_E = I_1 + I_{C4} = \frac{(1 + \beta_{F4})(1 + \beta_F) + \beta_{F4}}{(1 + \beta_{F4})(1 + \beta_F)} I_1. \quad (7)$$

The output current of the current switch transistor ( $Q_1$ ) is

$$I_{\text{out}} = \frac{I_E \beta_F}{1 + \beta_F} = \frac{\beta_F [(1 + \beta_{F4})(1 + \beta_F) + \beta_{F4}]}{(1 + \beta_{F4})(1 + \beta_F)(1 + \beta_F)} I_1. \quad (8)$$

If it is assumed that  $\beta_F = \beta_{F4}$ , then the output current of the current switch is

$$\begin{aligned} I_{\text{out}} &= \frac{\beta_F + 3\beta_F^2 + \beta_F^3}{1 + 3\beta_F + 3\beta_F^2 + \beta_F^3} I_1 \\ &= \frac{1}{1 + \frac{1 + 2\beta_F}{\beta_F + 3\beta_F^2 + \beta_F^3}} I_1. \end{aligned} \quad (9)$$

With the base current compensation circuit, the output current of the current switch could be approximated by

$$I_{\text{out}} = \frac{1}{1 + \frac{1 + 2\beta_F}{\beta_F + 3\beta_F^2 + \beta_F^3}} I_1 \approx \frac{1}{1 + \frac{2}{\beta_F^2}} I_1. \quad (10)$$

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